AMENDMENTS IN THE CLAIMS:

The following is a complete listing of all claims in the application, with an indication of the status of each:

Claim 1 (Currently Amended). An integrated circuit including an embedded memory and a built-in self-test arrangement including

means for storing test instructions ~~including means for~~ and discriminating ~~a source of a test command for~~ between performing manufacturing level ~~and~~ or board level testing and receiving test instructions provided from an external tester,

means for generating default test instructions **for performing manufacturing level or board level testing**, and

means for supplying said default test instructions **for performing manufacturing level or board level testing** to said means for storing test instructions,

wherein said means for generating default test instructions includes an initialization storage means.

Claim 2 (Currently Canceled).

Claim 3 (Currently Amended). An integrated circuit as recited in claim ~~2~~ 1, wherein said initialization storage means is a storage initialization module.

Claim 4 (Original). An integrated circuit as recited in claim 1, further including

means for activating said means for generating said default test instructions responsive to an absence of test instructions from an external tester.

Claim 5 (Original). An integrated circuit as recited in claim 1, further including

means for controlling a test operation, wherein said means for controlling a test operation includes means for supplying a control signal to an instruction storage controller and further includes said means for storing said test instructions.

Claim 6 (Original). An integrated circuit as received in claim 5, further including

means for activating said means for generating said default test instructions when only said control signal is supplied to said instruction storage controller.

Claim 7 (Original). An integrated circuit as recited in claim 1, wherein said means for generating default test instructions includes a memory for storing said default test instructions.

Claim 8 (Currently Amended). An electronic system including an integrated circuit having a built-in self-test arrangement therein, said integrated circuit including

means for storing test instructions ~~including means for~~ **and** discriminating ~~a source of a test command for~~ **between** performing manufacturing level ~~and~~ **or** board level testing and receiving test instructions provided from an external tester,

means for generating default test instructions **for performing manufacturing level or board level testing** in absence of instructions from an external tester, and

means for supplying said default test instructions **for performing manufacturing level or board level testing** to said means for storing test instructions**, wherein said means for generating default test instructions includes an initialization storage means.**

Claim 9 (Currently Canceled).

Claim 10 (Original). A system as recited in claim ~~9~~ **8**, wherein said initialization storage means is a storage initialization module.

Claim 11 (Original). A system as recited in claim 8, further including

means for activating said means for generating said default test instructions responsive to an absence of test instructions from an external tester.

Claim 12 (Currently Amended). ~~A method of performing system level tests on an electronic system including an integrated circuit having a built-in self-test (BIST) arrangement therein for performing manufacturing level and board level testing and including means for storing a test algorithm, said method comprising steps of~~

~~discriminating a source of a test command;~~

~~providing a system level test algorithm from said BIST arrangement in absence of instructions from an external tester;~~

~~transferring said system level test algorithm to said means for storing a test algorithm in said BIST arrangement, and~~

~~operating said BIST arrangement using said system level test algorithm~~

A system as recited in claim 8, further including

means for controlling a test operation, wherein said means for controlling a test operation includes means for supplying a control signal to an instruction storage controller and further includes said means for storing said test instructions.

Claim 13 (Original). A system as recited in claim 12, further including

means for activating said means for generating said default test instructions when only said control signal is supplied to said instruction storage controller.

Claim 14 (Original). A system as recited in claim 12, wherein said control signal is supplied from an external tester.

Claim 15 (Original). A system as recited in claim 12, wherein said control signal is supplied from within said system.

Claim 16 (Original). A system as recited in claim 8, wherein said means for generating default test instructions includes a memory for storing said default test instructions.

Claim 17 (Currently Amended). A method of performing system level tests on an

electronic system including an integrated circuit having a built-in self-test (BIST) arrangement therein for performing manufacturing level ~~and~~ **or** board level testing and including means for storing a test algorithm, said method comprising steps of

discriminating a source of a test command,

providing a system level test algorithm from said BIST arrangement **in absence of instructions from an external tester**,

transferring said system level test algorithm to said means for storing a test algorithm in said BIST arrangement, and

operating said BIST arrangement using said system level test algorithm.